UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/624,286	07/22/2003	Richard Louis Arndt	AUS920000364US2	7395

35525 7590 11/27/2006

IBM CORP (YA)
C/O YEE & ASSOCIATES PC
P.O. BOX 802333
DALLAS, TX 75380

EXAMINER	
PEYTON, TAMMARA R	
ART UNIT	**PAPER NUMBER**
2182	

DATE MAILED: 11/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/624,286	ARNDT ET AL.	
	Examiner	Art Unit	
	Tammara R. Peyton	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *8/17/06*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,7,8,12,13 and 17-23* is/are pending in the application.

4a) Of the above claim(s) *2,3,7,8,12 and 13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7,8,12,13 and 17-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/2/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 17, 18, 20, 22, and 23, are rejected under 35 U.S.C. 102(b) as being anticipated by Teodosiu, "Hive: Fault Containment for Shared-Memory Multiprocessor," SOSP '95.

As per claims 1, 17, 18, 20, 22, and 23, Teodosiu a teaches data processing system with programmable addressing, comprising:

multifunctional input/output devices (cells) in a logical partition environment (Abstract, Teodosiu teaches a protection domain partition environment for distributed system of kernels called cells, wherein the cells comprises a network of nodes. Each node includes a processor and a memory that is a portion of the shared main memory.)

control bits located in a memory, wherein the control bits allocate the multifunctional input/output devices into memory;

an address bus leading the control bits to locations for the multifunctional input/output devices; and

a programmable address control, wherein the programmable address control relocates individual functions. (See entire document, Figs. 3.1, 3.2, 3.3, 2.1)

Teodosiu teaches isolating the processors and the processor's memory and of each cell from the remaining processors of the network in an arrangement wherein a memory coupled to processors is partitioned to isolate user applications from one another (WAX) by having each user application of the single CPU/memory system serviced by its own respective operating system within a partition. When the system boots, each cell is assigned a range of nodes that it owns throughout execution and each cell controls (inherently via control bits (data)) an allocated portion of the shared address space and runs as an independent multiprocessor kernel (respective operating system).

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1, 17, 18, 20, 22, and 23, are rejected under 35 U.S.C. 102(e) as being anticipated by Bouchier et al., (US 6,684,343).

As per claims, 1, 17, 18, 20, 22, and 23, Bouchier teaches a data processing system with programmable addressing, comprising:

multifunctional input/output devices in a logical partition environment;

control bits located in a memory, wherein the control bits allocate the multifunctional input/output devices into memory;

an address bus leading the control bits to locations for the multifunctional input/output devices; and

a programmable address control, wherein the programmable address control relocates individual functions. (col. 1, lines 58-col. 13)

Bouchier teaches a logical partition system environment having a group of cabinets wherein each cabinet contains a cell board. The cell board has a plurality of system CPUs/OS together with system memory with an I/O connection controller (PCI, etc.). Each partition must have at least enough I/O attached to its cell board(s) to be able to boot the OS and each cell has a partition to communicate with one another and software or firmware running on a partition can operate the I/O controllers to transfer data between system memory and external disks, networks, and multifunctional I/O devices. The multiple copies of the OS are run independently of each other and control bits are utilized for allocation for each instance of the OS. Further, each partition that has its own cell boards with processors and memory and connected I/O are isolated between different applications.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 19 and 21 rejected under 35 U.S.C. 103(a) as being unpatentable over Teodosiu, "Hive: Fault Containment for Shared-Memory Multiprocessor," SOSP '95, or Bouchier et al., and Nale (5,987,581), filed under prior art, 4/2/04.

As per claims 19 and 21, Hive and Bouchier both disclose a method of a programmable address control for resource reallocation of services for multifunctional devices and protecting/isolating partitions running multiple instances of operating systems, however, Hive nor Bouchier specifically teach inserting an inverter on an address bus for the multifunctional input/output device. Nonetheless, Nale teaches selectively inverting the state of an address line on an address bus that includes a selectable inverter element and a control circuit. This method taught by Nale prevents two blocks from accessing the same location in the system memory. (Nale, cols.1-9) Therefore, it would have been obvious to one of ordinary skill at the time the invention was made to implement the method of inverting the state of an address line on an address bus into Hive and Bouchier partition environment system because doing to would add and expand the flexibility of both systems and further enhance the

protection/isolation of partitions by preventing certain partitions from accessing similar memory locations.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tammara Peyton whose telephone number is (571) 272-4157. The examiner can normally be reached between 6:30 - 4:00 from Monday to Thursday, (I am off every first Friday), and 6:30-3:00 every second Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300. Any inquiry of a general nature of relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-2100.

Mailed responses to this action should be sent to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231.

Faxes for Official/formal (After Final) communications or for informal or draft communications (please label "PROPOSED" or "DRAFT") sent to:

(571) 273-8300

Hand-delivered responses should be brought to:
USTPO, Randolph Building, Customer Service Window
401 Dulany Street
Alexandria, VA 22314.

TAMMARA PEYTON
PRIMARY EXAMINER

Tammara Peyton
September 26, 2006